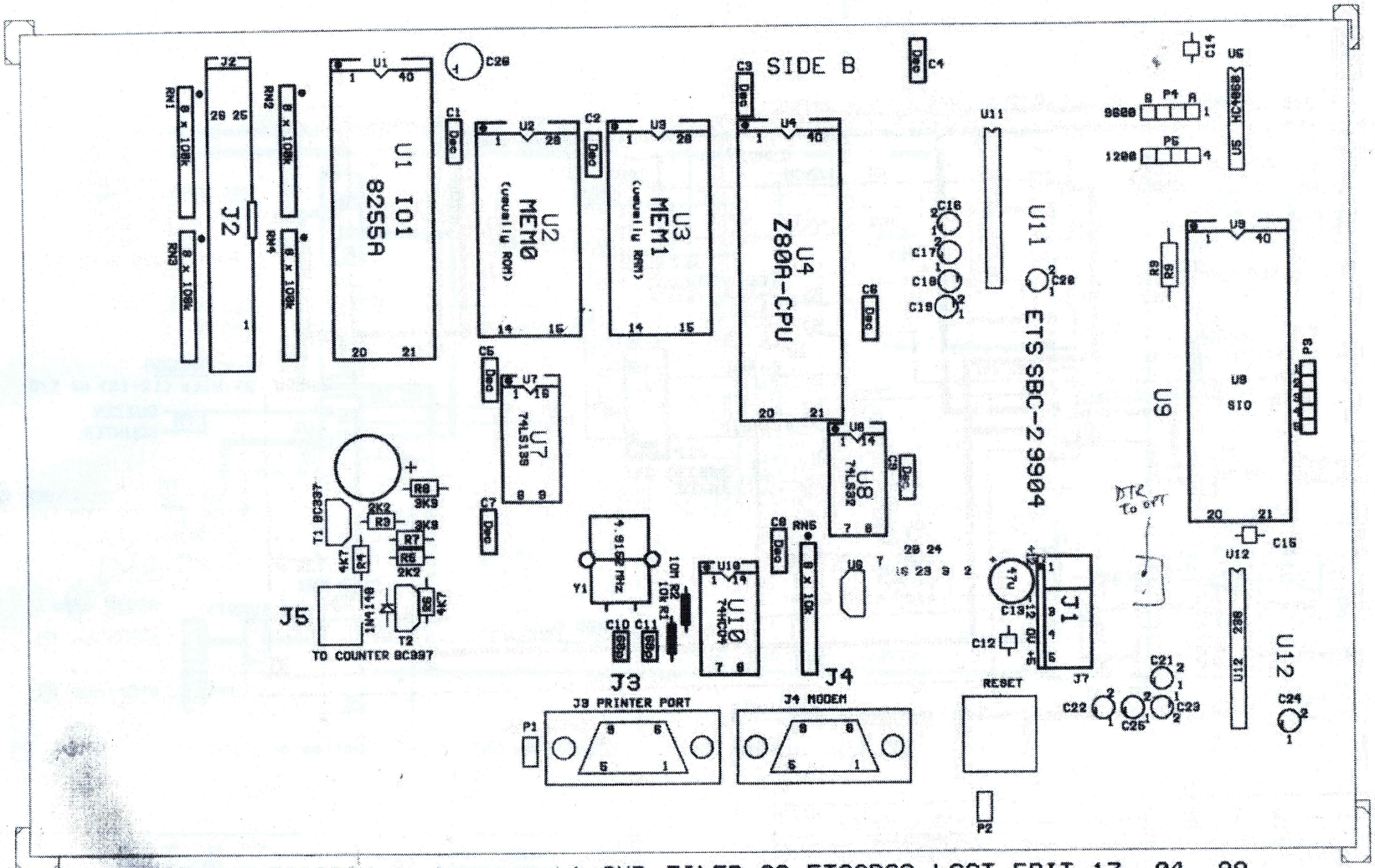
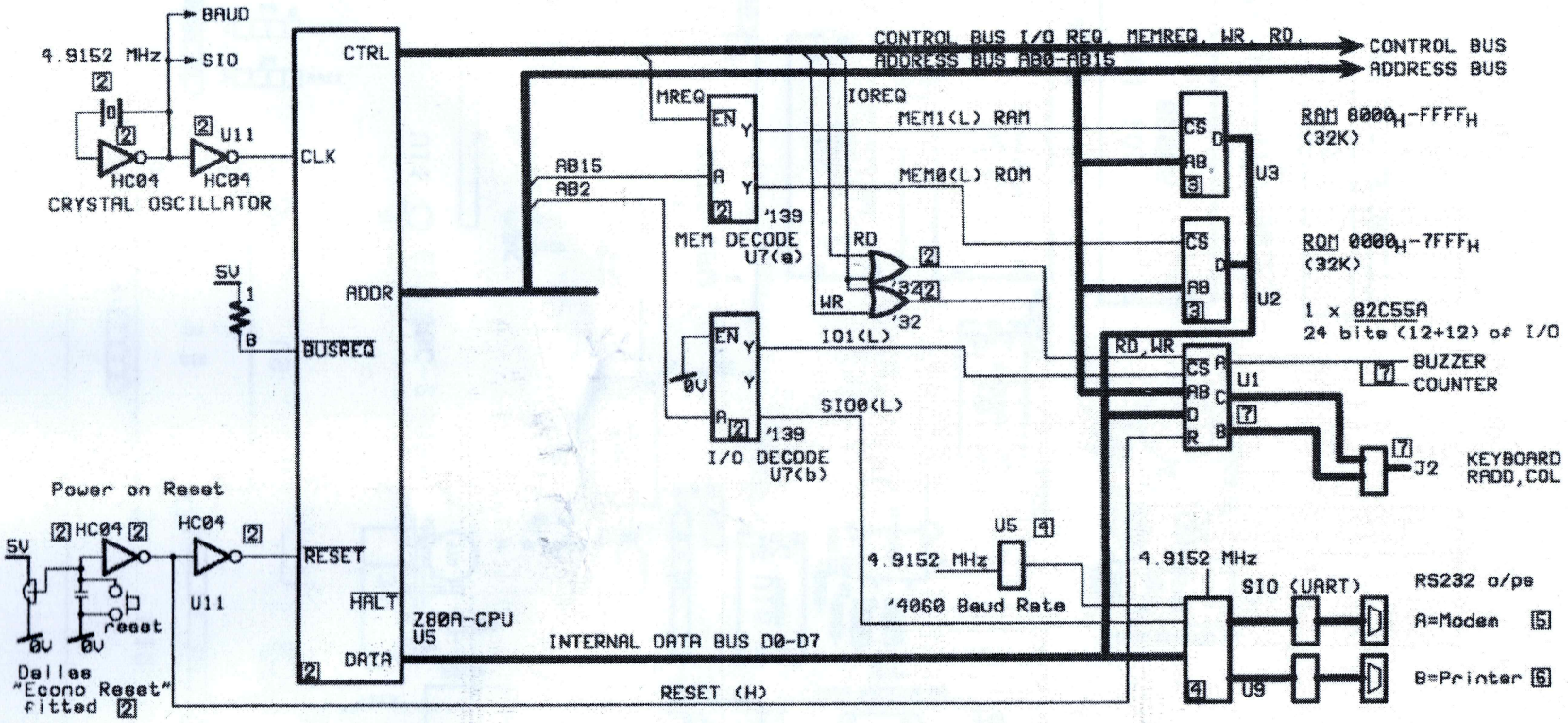
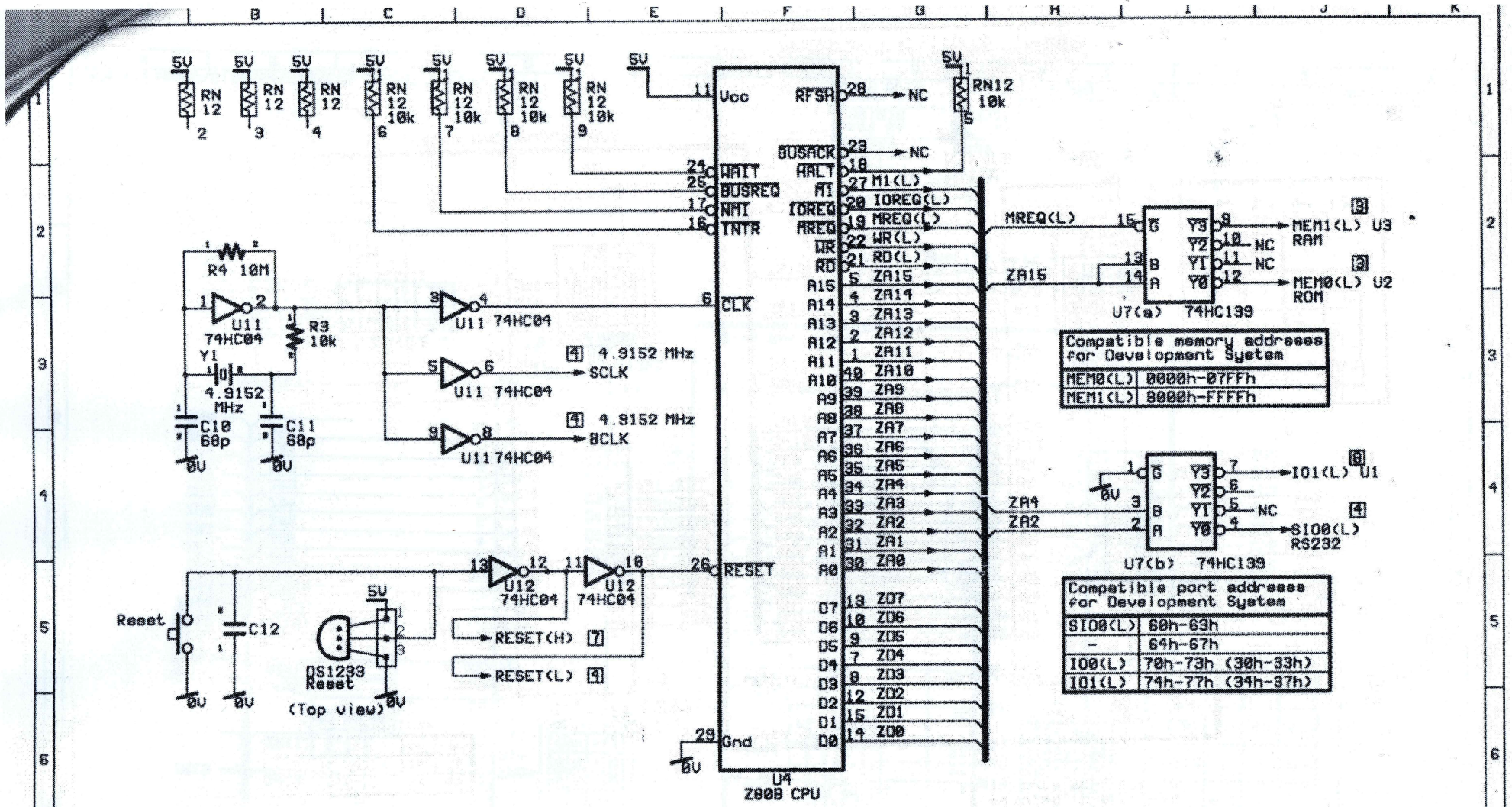


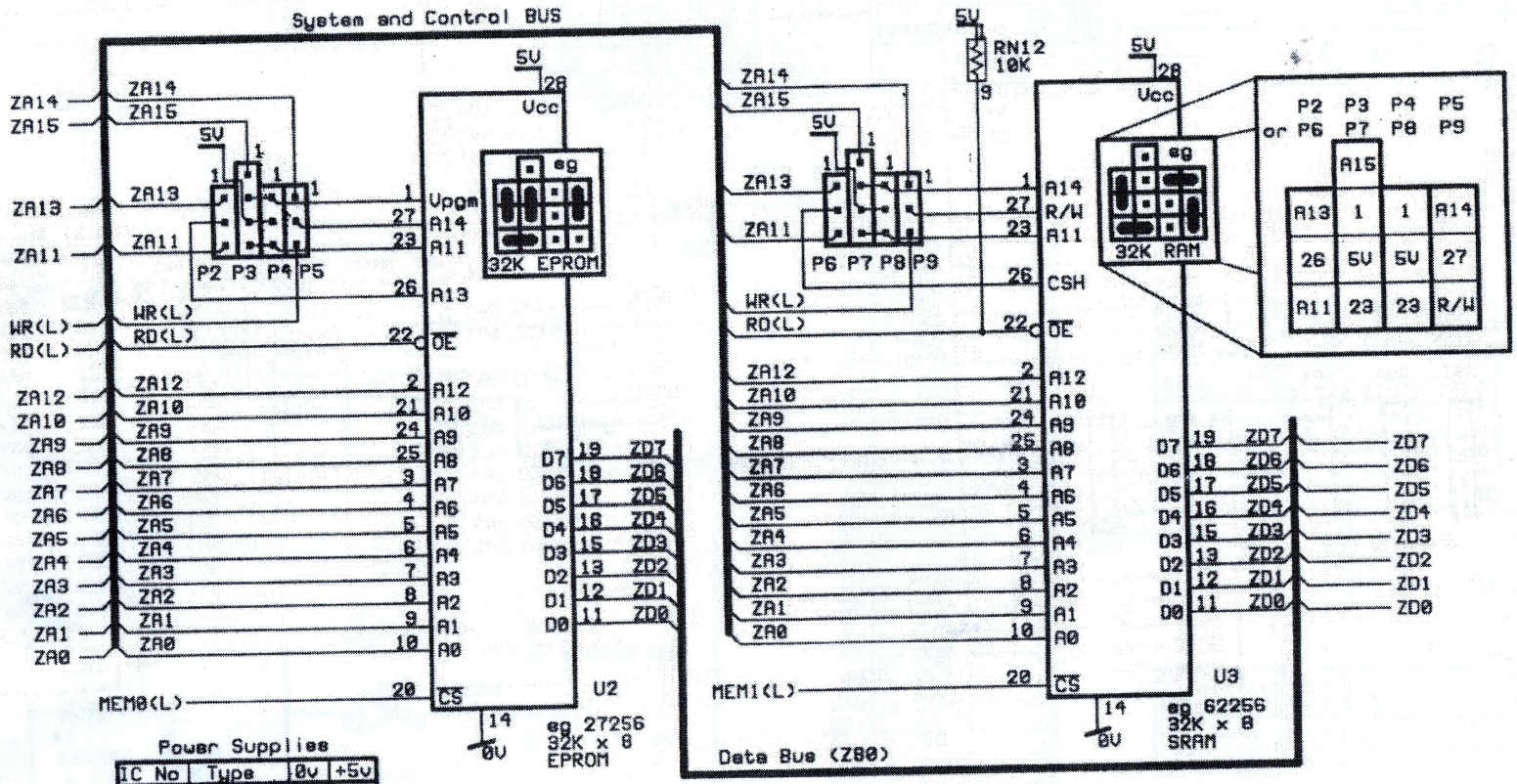
ASSEMBLY DIAGRAM (not for pcb) AND FILED AS ETSSBC3 LAST EDIT 17. 04. 99.
OUTER SILK SCREEN FOR SIDE B (WHITE)



File: LB5SBC_1.SCH	E & T S
Started: 890525 960731	E & T S Lottery Controller SBC Board
Last Edit: 951004 981021 990414	Block Diagram
Drawn by: SD45 0D20	(c) 1999 E & T S — Sheet 1/8

ADocs\EasyPc\Clients\ETS\ETS_LB5\SBC1_LB5 — Board Ref: ETS SBC3 9904


RN 12
RN12 10k
R4 10M
R3 10k
Y1
4.9152 MHz
C10 68p
C11 68p
C12
Reset
DS1233 Reset
(Top view)
U11 74HC04
U12 74HC04
U4 Z80B CPU
Vcc
Gnd
CLK
RESET
WAIT
BUSREQ
NMI
INTR
RFSH
BUSACK
HALT
M1
IOREQ
MREQ
WR
RD
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
D7
D6
D5
D4
D3
D2
D1
D0
NC
M1(L)
IOREQ(L)
MREQ(L)
WR(L)
RD(L)
ZA15
ZA14
ZA13
ZA12
ZA11
ZA10
ZA9
ZA8
ZA7
ZA6
ZA5
ZA4
ZA3
ZA2
ZA1
ZA0
ZD7
ZD6
ZD5
ZD4
ZD3
ZD2
ZD1
ZD0
4.9152 MHz
SCLK
BCLK
RESET(H)
RESET(L)
U7(a) 74HC139
U7(b) 74HC139
MEM1(L) U3 RAM
MEM0(L) U2 ROM
IO1(L) U1
SIO0(L) RS232
Compatible memory addresses for Development System
MEM0(L) 0000h-07FFh
MEM1(L) 8000h-FFFFh
Compatible port addresses for Development System
SIO0(L) 60h-63h
- 64h-67h
IO0(L) 70h-73h (30h-33h)
IO1(L) 74h-77h (34h-37h)
Power Supplies
IC No | Type | 0v | +5v
U4 | Z80B-CPU | 26 | 11
U11 | 74HC04 | 7 | 14
U7 | 74HC139 | 8 | 16
U8 | 74HC32 | 7 | 14
File: L85SBC_2.SCH
Started: 890525 980204
Last Edit: 960731 981016 990414
Drawn by: 6D05 0J25 0D20
E & T S
E & T S Lottery System SBC Board
Z80A-CPU, Decoders
(c)1999 E & T S
Sheet 2/8
ADocs\EasyPC\Clients\ETS\ETS_L85\SBC1_L85\



Power Supplies

IC No	Type	0v	+5v
U2	27256	14	28
U3	62256	14	28

U3 in this application is mounted in a Dallas Smart Socket DS1216C

File: LB5SBC_3.SCH	E & T S
Started: 990525 980204	E & T S Lottery System SBC Board
Last Edit: 981016 990414	Memory
Drawn by: SD10 0J25 0D10	(c)1999 E & T S — Sheet 3/8

ADocs\EasyPC\Clients\ETS\ETS_LB5\SBC1_LB5\

Patch area for ROM/RAMs SBC-1

(Version 8811)

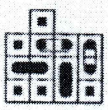
P2	P3	P4	P5
	A15		
A13	1	1	A14
26	5V	5V	27
A11	23	23	R/W

P6	P7	P8	P9
	A15		
A13	1	1	A14
26	5V	5V	27
A11	23	23	R/W

Represents JLINK connection
Represents position for spare JLINK

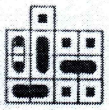
ROM

2K (2716)

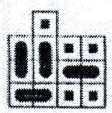


4K (2732)

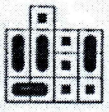
PIN 26?
8K (2764)



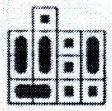
16K (27128)



32K (27256)

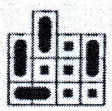


64K (27512)



Appears as a 32K x 8 EPROM (Code in 2nd half)

64K (27512)

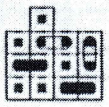


Appears as a 64K x 8 EPROM Do not fit any RAM

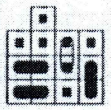
Last Revision 12/04/89

RAM

2K (6116)

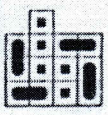


8K (6264)



connect RAM pin 1 to +5 volts when using Dallas 1216 RTC

32K (62256)

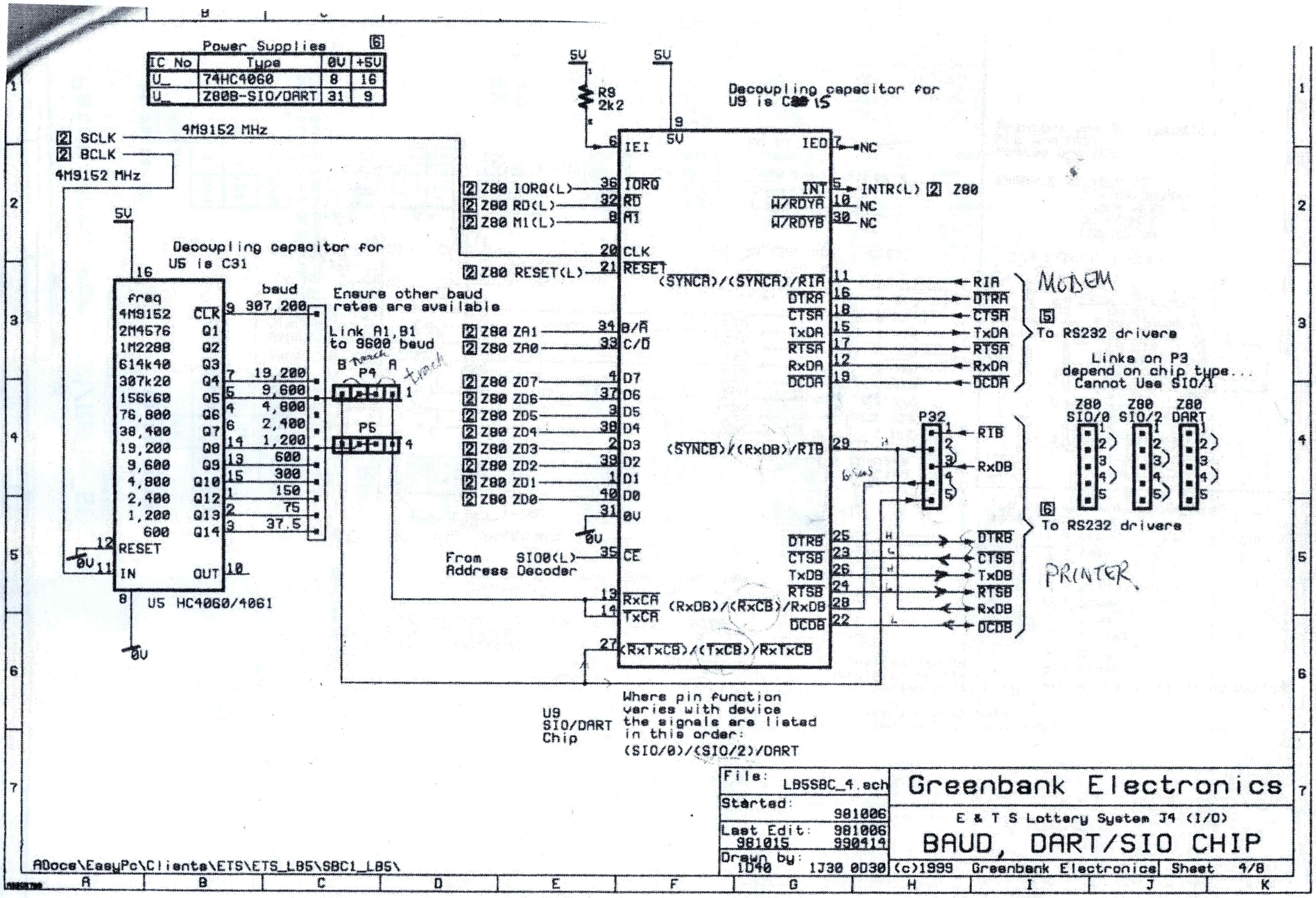


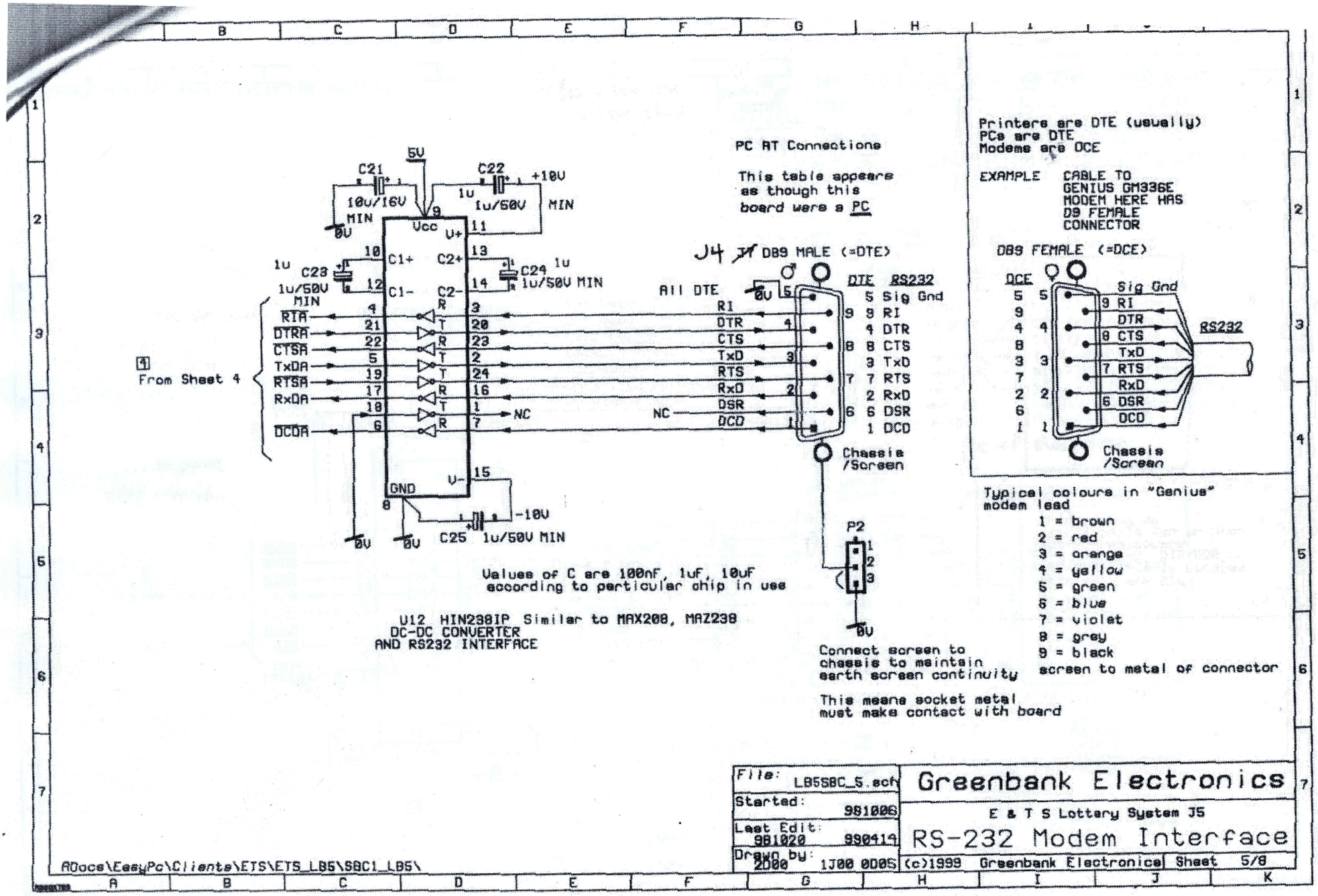
	Pins				
	Size	1	23	26	27	
As ROM Socket	2K	X	Vpp	Vcc	X	
	4K	X	A11	Vcc	X	
	8K	5V	A11	NC	PGM(L)	
	16K	5V	A11	A13	PGM(L)	
	32K	5V	A11	A13	A14	
	64K	5V	A11	A13	A14	(Appears as 32K ROM)
	64K	A15	A11	A13	A14	(Appears as 64K ROM)
As RAM Socket	2K	X	R/W	Vcc	X	
	8K	X	A11	CSH	R/W	Pin 1 to +5 volts for Dallas 1216
	32K	A14	A11	A13	R/W	

Drawn	JHP
Date	890609
Scale	—

Interak

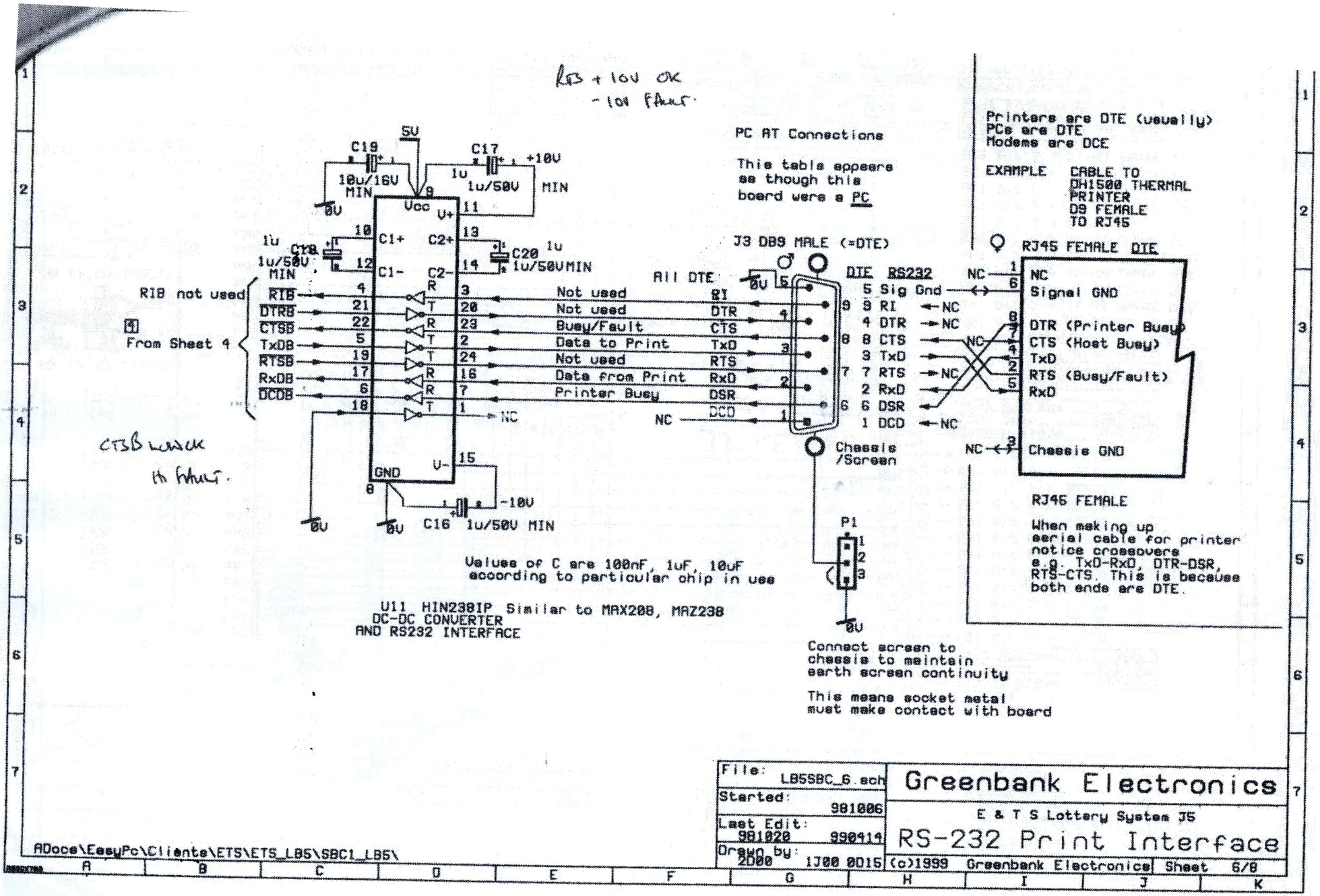
SBC-1 MEMORY SELECTION LINKS

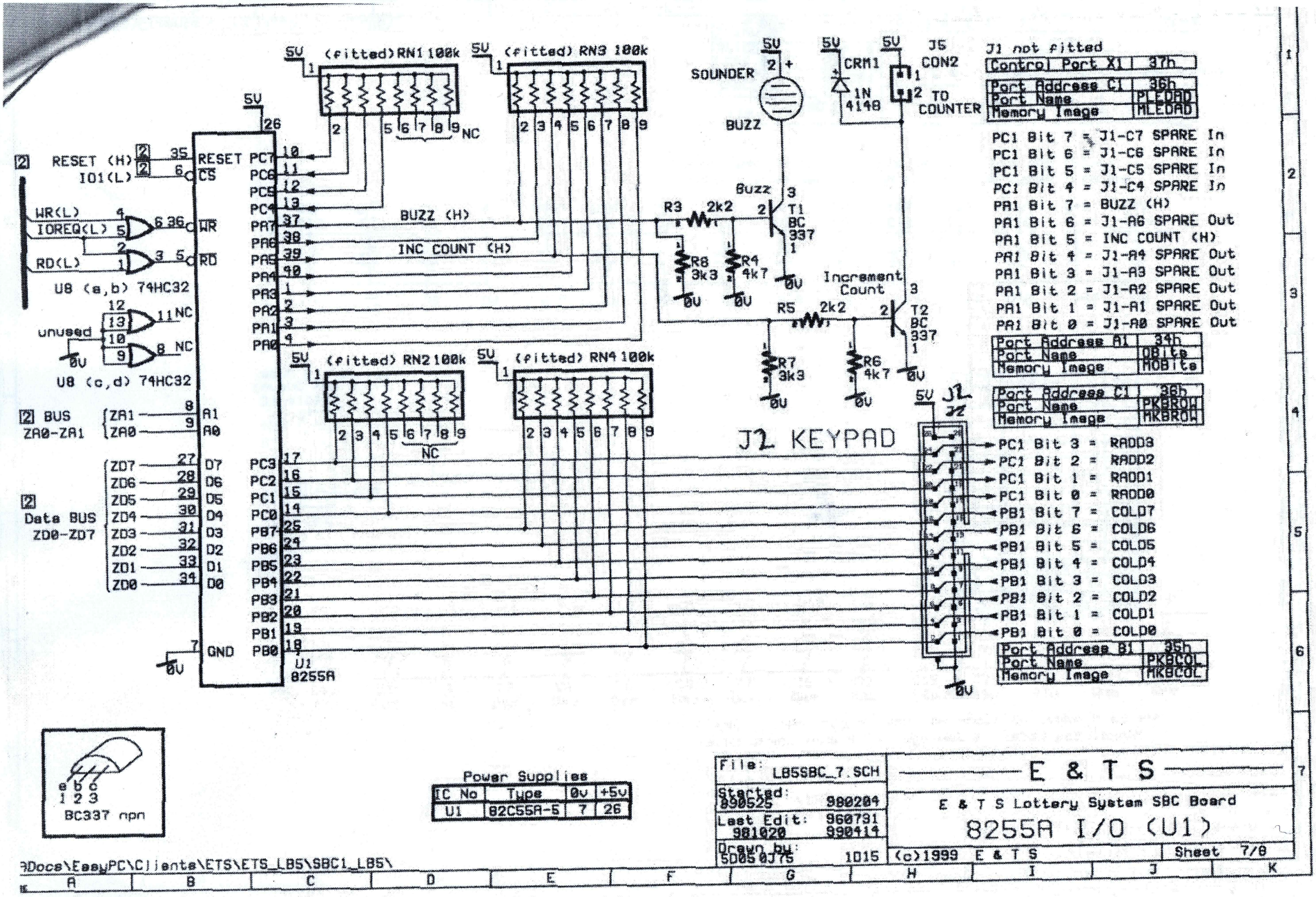

Power Supplies [6]
IC No | Type | 0V | +5V
U_ | 74HC4060 | 8 | 16
U_ | Z80B-SIO/DART | 31 | 9
[2] SCLK
[2] BCLK
4M9152 MHz
4M9152 MHz
5V
R9 2k2
Decoupling capacitor for U9 is C[illegible]15
Decoupling capacitor for U5 is C31
freq
4M9152 CLK
2M4576 Q1
1M2288 Q2
614k40 Q3
307k20 Q4
156k60 Q5
76,800 Q6
38,400 Q7
19,200 Q8
9,600 Q9
4,800 Q10
2,400 Q12
1,200 Q13
600 Q14
RESET
IN
OUT
U5 HC4060/4061
baud
307,200
19,200
9,600
4,800
2,400
1,200
600
300
150
75
37.5
Ensure other baud rates are available
Link A1,B1 to 9600 baud
P4
P5
B
A
track
[2] Z80 IORQ(L)
[2] Z80 RD(L)
[2] Z80 M1(L)
[2] Z80 RESET(L)
[2] Z80 ZA1
[2] Z80 ZA0
[2] Z80 ZD7
[2] Z80 ZD6
[2] Z80 ZD5
[2] Z80 ZD4
[2] Z80 ZD3
[2] Z80 ZD2
[2] Z80 ZD1
[2] Z80 ZD0
From Address Decoder SIO0(L)
IEI
IEO
NC
IORQ
RD
M1
CLK
RESET
B/A
C/D
D7
D6
D5
D4
D3
D2
D1
D0
0V
CE
RxCA
TxCA
(RxTxCB)/(TxCB)/RxTxCB
INT
W/RDYA
W/RDYB
INTR(L) [2] Z80
(SYNCA)/(SYNCA)/RIA
DTRA
CTSA
TxDA
RTSA
RxDA
DCDA
(SYNCB)/(RxDB)/RIB
(RxDB)/(RxCB)/RxDB
DTRB
CTSB
TxDB
RTSB
RxDB
DCDB
MODEM
[5] To RS232 drivers
Links on P3 depend on chip type... Cannot Use SIO/1
Z80 SIO/0
Z80 SIO/2
Z80 DART
P32
RIB
RxDB
[6] To RS232 drivers
PRINTER
U9 SIO/DART Chip
Where pin function varies with device the signals are listed in this order:
(SIO/0)/(SIO/2)/DART
File: LB5SBC_4.sch
Started: 981006
Last Edit: 981015 981006 990414
Drawn by: 1D40 1J30 0D30
Greenbank Electronics
E & T S Lottery System J4 (I/O)
BAUD, DART/SIO CHIP
(c)1999 Greenbank Electronics
Sheet 4/8
ADocs\EasyPc\Clients\ETS\ETS_LB5\SBC1_LB5\

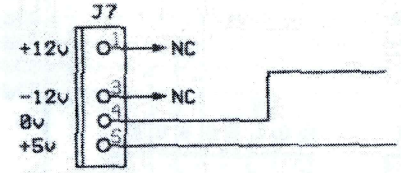


File: LB5SBC_5.sch	Greenbank Electronics
Started: 981006	E & T S Lottery System J5
Last Edit: 981020 990419	RS-232 Modem Interface
Drawn by: 2000 1J00 0D05	(c)1999 Greenbank Electronics Sheet 5/8

ADocs\EasyPc\Clients\ETS\ETS_LB5\SBC1_LB5\


RS3 +10V OK
-10V FAULT
5V
C19
10u/16V MIN
C17
1u
+10V
1u/50V MIN
0V
Vcc
V+
C1+
C2+
C1-
C2-
C18
1u/50V MIN
C20
1u/50V MIN
RIB not used
From Sheet 4
RIB
DTRB
CTSB
TxDB
RTSB
RxDB
DCDB
Not used
Not used
Busy/Fault
Data to Print
Not used
Data from Print
Printer Busy
NC
GND
V-
-10V
C16 1u/50V MIN
CTSB LOCK IN FAULT.
PC AT Connections
This table appears as though this board were a PC
J3 DB9 MALE (=DTE)
All DTE
DIE RS232
5 Sig Gnd
9 RI
4 DTR
8 CTS
3 TxD
7 RTS
2 RxD
6 DSR
1 DCD
Chassis /Screen
RJ45 FEMALE DIE
NC
Signal GND
DTR (Printer Busy)
CTS (Host Busy)
TxD
RTS (Busy/Fault)
RxD
Chassis GND
Printers are DTE (usually)
PCs are DTE
Modems are DCE
EXAMPLE CABLE TO DH1500 THERMAL PRINTER D9 FEMALE TO RJ45
RJ45 FEMALE
When making up serial cable for printer notice crossovers e.g. TxD-RxD, DTR-DSR, RTS-CTS. This is because both ends are DTE.
Values of C are 100nF, 1uF, 10uF according to particular chip in use
U11 HIN238IP Similar to MAX208, MAZ238
DC-DC CONVERTER AND RS232 INTERFACE
P1
Connect screen to chassis to maintain earth screen continuity
This means socket metal must make contact with board
File: LB5SBC_6.sch
Started: 981006
Last Edit: 981020 990414
Drawn by: 2000 1J00 0D15
Greenbank Electronics
E & T S Lottery System J5
RS-232 Print Interface
(c)1999 Greenbank Electronics
Sheet 6/8
ADocs\EasyPc\Clients\ETS\ETS_LB5\SBC1_LB5\

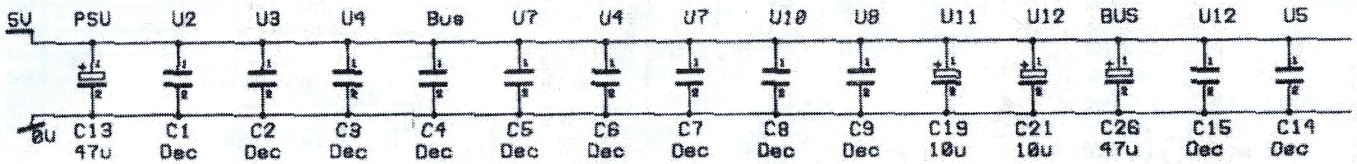

5V
(fitted) RN1 100k
(fitted) RN3 100k
(fitted) RN2 100k
(fitted) RN4 100k
SOUNDER
BUZZ
CRM1
1N 4148
J5
CON2
TO COUNTER
J1 not fitted
Control Port X1 37h
Port Address C1 36h
Port Name PLEDAD
Memory Image MLEDAD
PC1 Bit 7 = J1-C7 SPARE In
PC1 Bit 6 = J1-C6 SPARE In
PC1 Bit 5 = J1-C5 SPARE In
PC1 Bit 4 = J1-C4 SPARE In
PA1 Bit 7 = BUZZ (H)
PA1 Bit 6 = J1-A6 SPARE Out
PA1 Bit 5 = INC COUNT (H)
PA1 Bit 4 = J1-A4 SPARE Out
PA1 Bit 3 = J1-A3 SPARE Out
PA1 Bit 2 = J1-A2 SPARE Out
PA1 Bit 1 = J1-A1 SPARE Out
PA1 Bit 0 = J1-A0 SPARE Out
Port Address A1 34h
Port Name QBits
Memory Image MQBits
Port Address C1 38h
Port Name PKBROW
Memory Image MKBROW
Port Address B1 35h
Port Name PKBCOL
Memory Image MKBCOL
RESET (H)
IO1(L)
RESET
CS
WR(L)
IOREQ(L)
RD(L)
WR
RD
U8 (a,b) 74HC32
unused
U8 (c,d) 74HC32
BUS ZA0-ZA1
ZA1
ZA0
A1
A0
Data BUS ZD0-ZD7
ZD7
ZD6
ZD5
ZD4
ZD3
ZD2
ZD1
ZD0
D7
D6
D5
D4
D3
D2
D1
D0
GND
PC7
PC6
PC5
PC4
PA7
PA6
PA5
PA4
PA3
PA2
PA1
PA0
PC3
PC2
PC1
PC0
PB7
PB6
PB5
PB4
PB3
PB2
PB1
PB0
U1
8255A
BUZZ (H)
INC COUNT (H)
NC
R3 2k2
R8 3k3
R4 4k7
R5 2k2
R7 3k3
R6 4k7
Buzz
T1 BC 337
Increment Count
T2 BC 337
J2
J2 KEYPAD
PC1 Bit 3 = RADD3
PC1 Bit 2 = RADD2
PC1 Bit 1 = RADD1
PC1 Bit 0 = RADD0
PB1 Bit 7 = COLD7
PB1 Bit 6 = COLD6
PB1 Bit 5 = COLD5
PB1 Bit 4 = COLD4
PB1 Bit 3 = COLD3
PB1 Bit 2 = COLD2
PB1 Bit 1 = COLD1
PB1 Bit 0 = COLD0
e b c
1 2 3
BC337 npn
Power Supplies
IC No | Type | 0v | +5v
U1 | 82C55A-5 | 7 | 26
File: L85SBC_7.SCH
Started: 980204
Last Edit: 960731 981020 990414
Drawn by: SDOS OJTS 1015
E & T S
E & T S Lottery System SBC Board
8255A I/O (U1)
(c)1999 E & T S
Sheet 7/8
C:\Docs\EasyPC\Clients\ETS\ETS_L85\SBC1_L85\



J7 fitted
(wrong way on
many ETS boards)

Power Supplies

IC No	Type	0v	+5v
U8	74HC32	7	14
U7	74HC139	8	16
U12	74HC14	7	14



Check - some may already be shown on other diagrams
also check ends 1, 2, against finished pcb layout

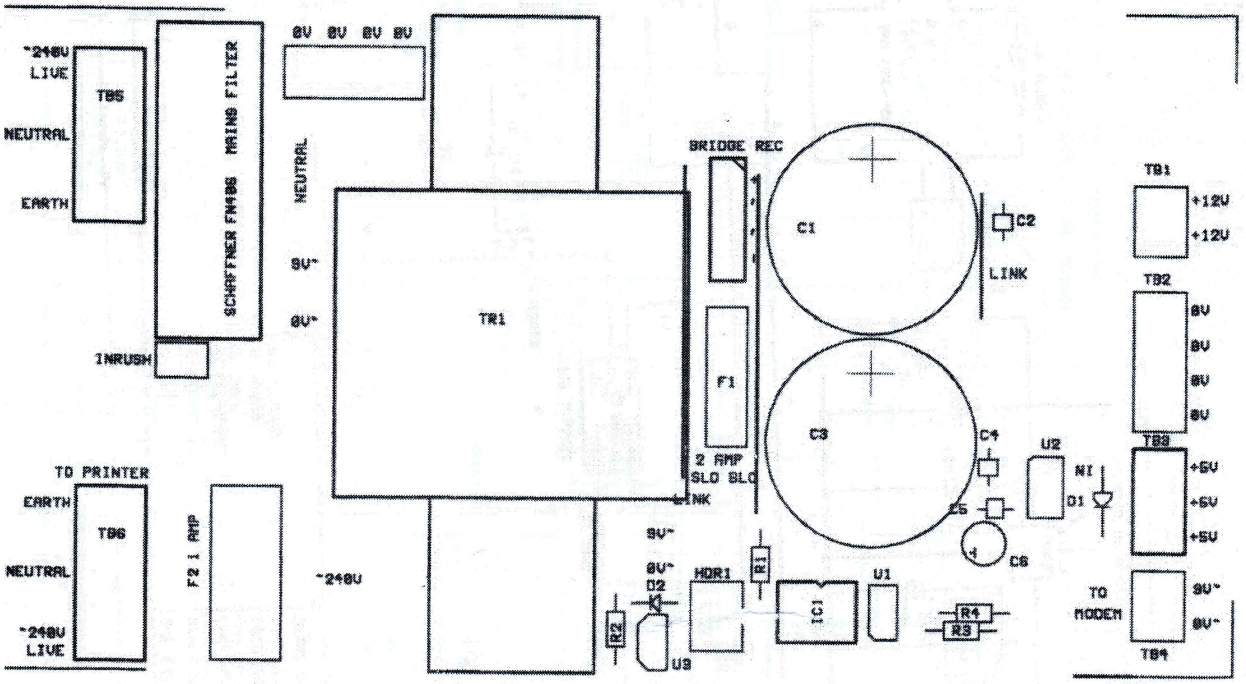
File: LBSSBC_8.SCH	E & T S
Started: 960731 090525 980204	E & T S Lottery System SBC Board
Last Edit: 980204 981021 990414	Power
Drawn by: 5D45 0725 0D10	(c)1999 E & T S — Sheet 8/8

RDoce\EasyPc\Clients\ETS\ETS_LB5\SBC1_LB5\

FILED AS POWER

POWER SUPPLY

LAST EDIT 13.09.99

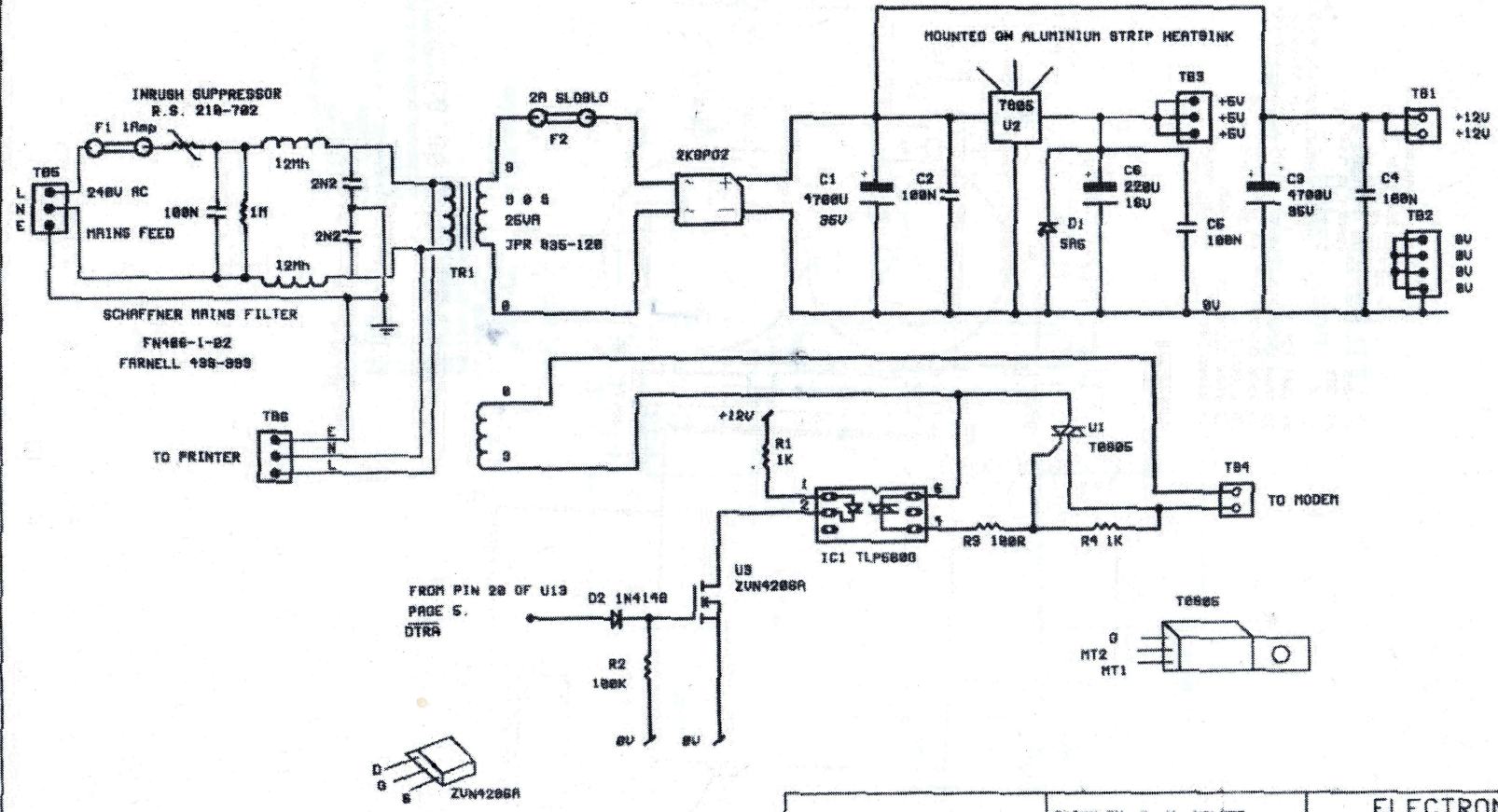


COMPONENTS

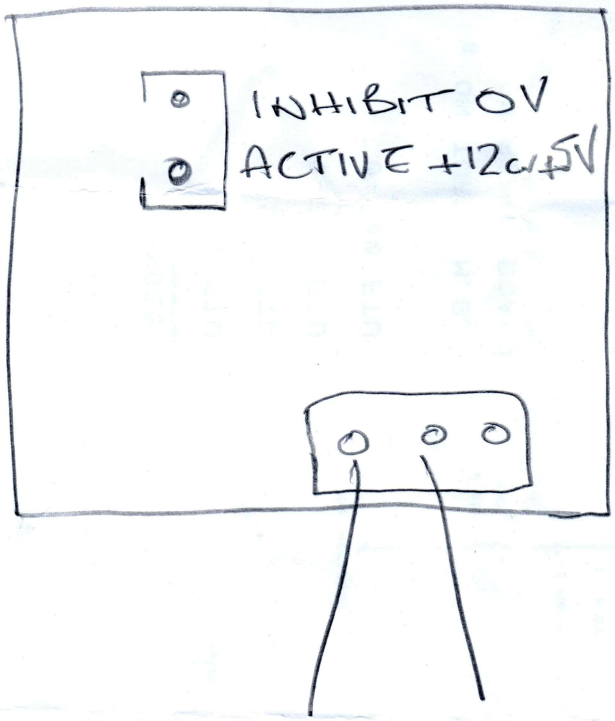
C1 4700U 35V
C2 100N DECOUPLER
C3 4700U 35V
C4 100N DECOUPLER
C5 100N DECOUPLER
C6 220U 16V

R1 1K
R2 150K
R3 100R
R4 1K

BR REC 2KBP02
U2 7805
F1 2A SLOBLO
F2 1AMP QUICK BLO
MAINS FILTER FARNELL 439-389 SCHAFFNER FN406
RAPID 26-4520
TR1 TRANSFORMER S-8-9 25VA RAPID 99-0296
D1 SR5 JPR 035-120
INRUSH RS 218-782
IC1 TLP560
D2 1N4148
U3 ZVN4206A
HDR1 LUMBERG 2WAY

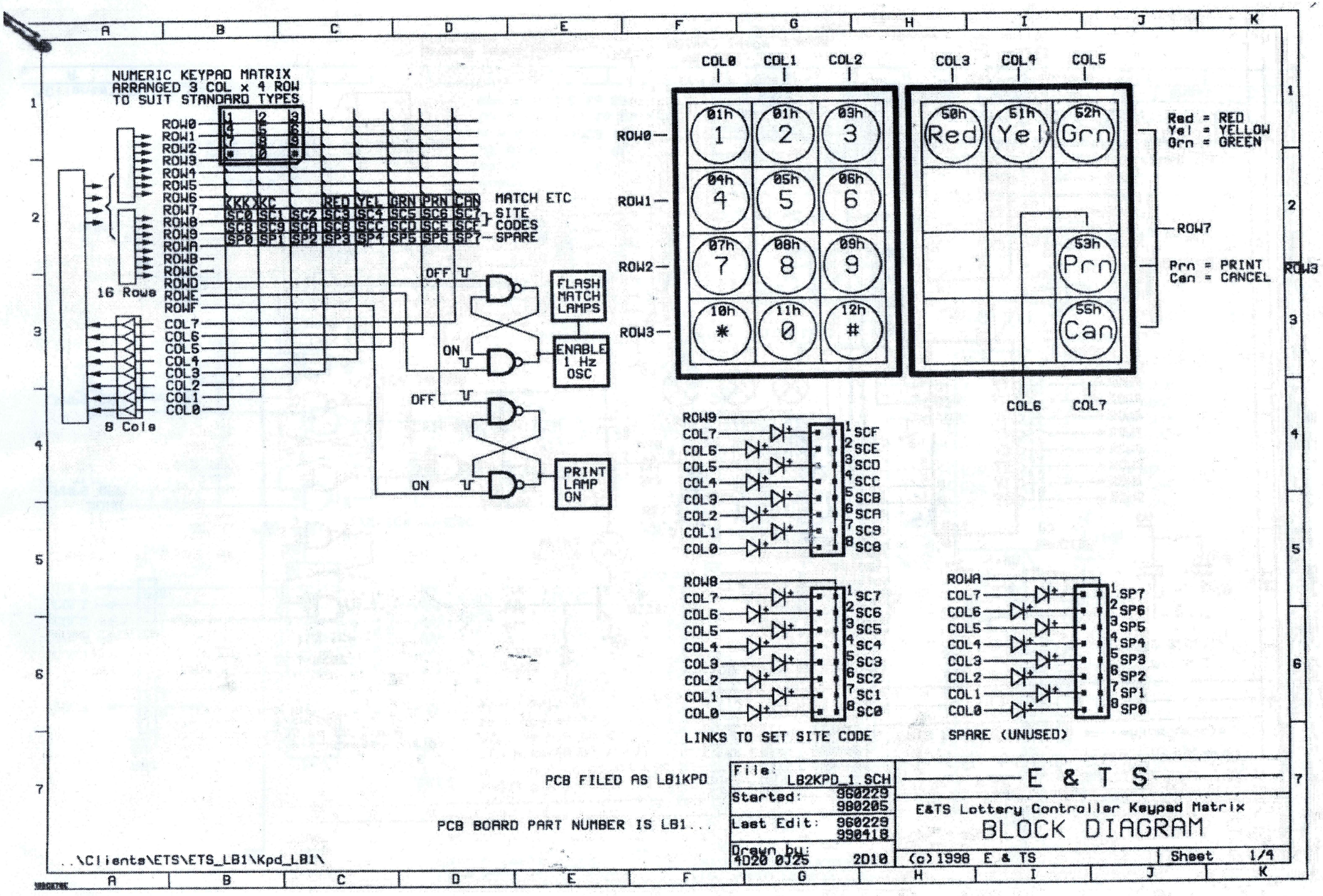


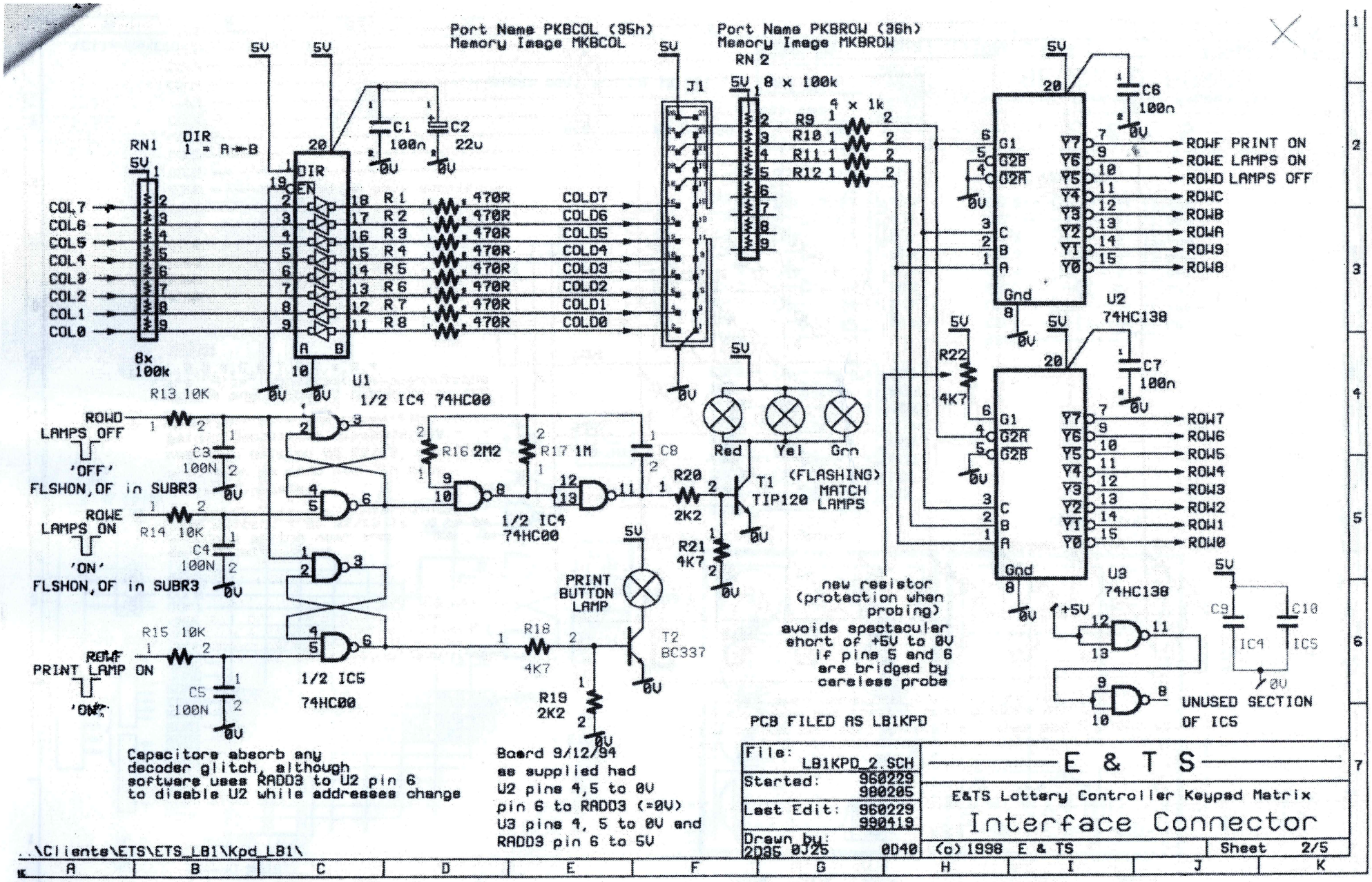
IC1 TLP508G U1 T805SM U2 7805 U3 ZVN4206A	DRAWN BY J. W. WALKER	ELECTRONIC & TECH SERVICES Ltd
	DATE STARTED 24. 02. 98.	CIRCUIT FOR LOTTERY POWER SUPPLY
	LAST EDIT 18. 03. 98.	
	SCH FILED AS PSUPPLYN PCB FILED AS POWER	©1996 ELECTRONIC & TECHNICAL SERVICES LTD — 1 OF 1

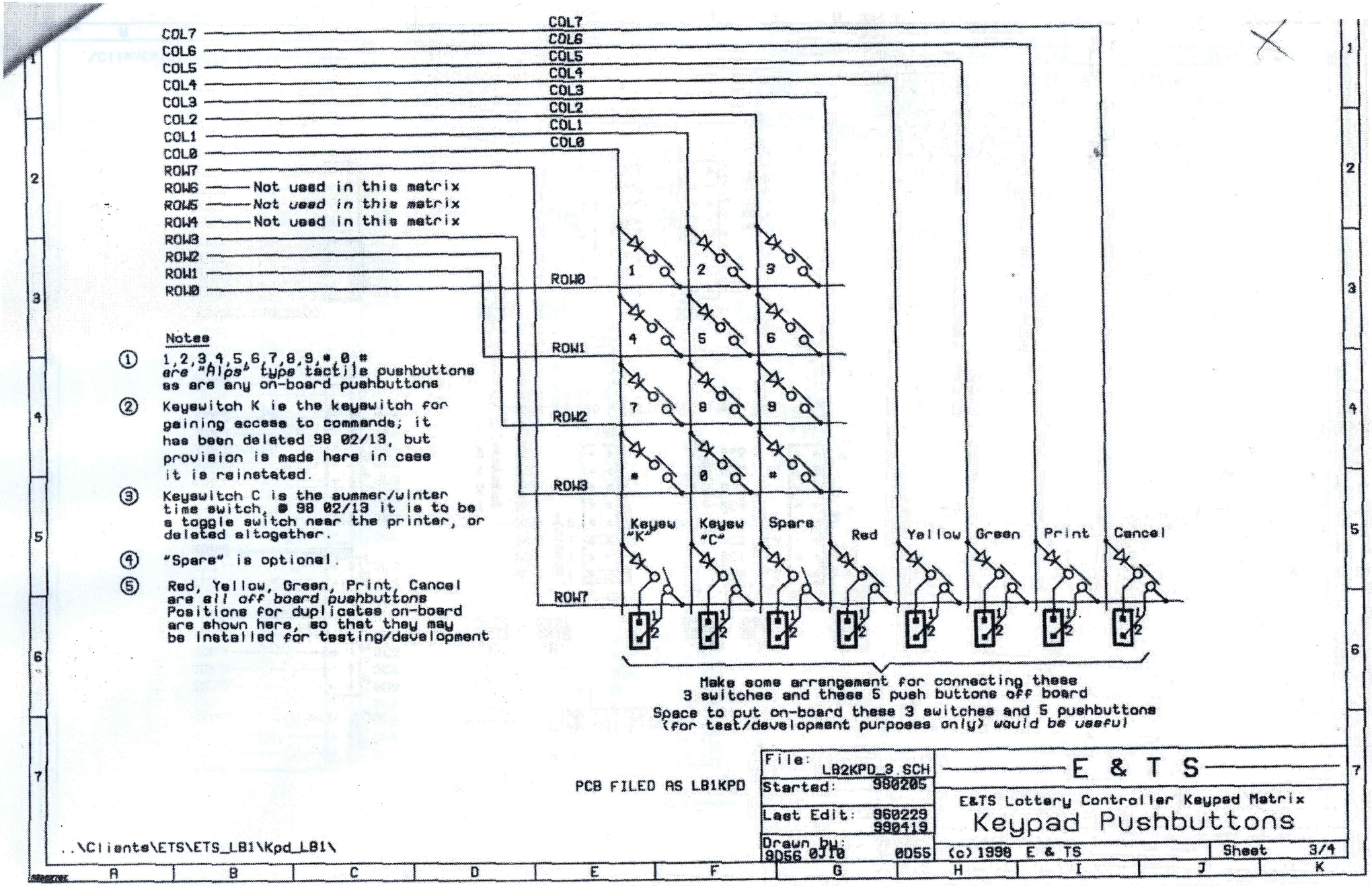


9V AC OUT ACTIVE

NO OUTPUT INHIBIT OV


NUMERIC KEYPAD MATRIX
ARRANGED 3 COL x 4 ROW
TO SUIT STANDARD TYPES
ROW0
ROW1
ROW2
ROW3
ROW4
ROW5
ROW6
ROW7
ROW8
ROW9
ROWA
ROWB
ROWC
ROWD
ROWE
ROWF
16 Rows
COL7
COL6
COL5
COL4
COL3
COL2
COL1
COL0
8 Cols
MATCH ETC
SITE CODES
SPARE
OFF
ON
FLASH MATCH LAMPS
ENABLE 1 Hz OSC
PRINT LAMP ON
COL0 COL1 COL2 COL3 COL4 COL5
01h 1
01h 2
03h 3
04h 4
05h 5
06h 6
07h 7
08h 8
09h 9
10h *
11h 0
12h #
50h Red
51h Yel
52h Grn
53h Prn
55h Can
Red = RED
Yel = YELLOW
Grn = GREEN
ROW7
Prn = PRINT
Can = CANCEL
COL6
COL7
SCF
SCE
SCD
SCC
SCB
SCA
SC9
SC8
LINKS TO SET SITE CODE
SC7
SC6
SC5
SC4
SC3
SC2
SC1
SC0
SPARE (UNUSED)
SP7
SP6
SP5
SP4
SP3
SP2
SP1
SP0
PCB FILED AS LB1KPD
PCB BOARD PART NUMBER IS LB1...
File: LB2KPD_1.SCH
Started: 960229 980205
Last Edit: 960229 990418
Drawn by: 4D20 0J25 2D10
E & T S
E&TS Lottery Controller Keypad Matrix
BLOCK DIAGRAM
(c)1998 E & TS
Sheet 1/4
..\Clients\ETS\ETS_LB1\Kpd_LB1\


Port Name PKBCOL (35h)
Memory Image MKBCOL
Port Name PKBROW (36h)
Memory Image MKBROW
RN 2
8 x 100k
4 x 1k
RN1
DIR
1 = A→B
8x
100k
U1
1/2 IC4 74HC00
U2
74HC138
U3
74HC138
COL7
COL6
COL5
COL4
COL3
COL2
COL1
COL0
COLD7
COLD6
COLD5
COLD4
COLD3
COLD2
COLD1
COLD0
470R
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
C1
100n
C2
22u
C6
C7
C8
C3
C4
C5
R13 10K
R14 10K
R15 10K
R16 2M2
R17 1M
R18
4K7
R19
2K2
R20
2K2
R21
4K7
R22
4K7
ROWF PRINT ON
ROWE LAMPS ON
ROWD LAMPS OFF
ROWC
ROWB
ROWA
ROW9
ROW8
ROW7
ROW6
ROW5
ROW4
ROW3
ROW2
ROW1
ROW0
ROWD
LAMPS OFF
'OFF'
FLSHON,OF in SUBR3
ROWE
LAMPS ON
'ON'
FLSHON,OF in SUBR3
ROWF
PRINT LAMP ON
'ON'
Red
Yel
Grn
T1
TIP120
(FLASHING)
MATCH
LAMPS
PRINT
BUTTON
LAMP
T2
BC337
1/2 IC4
74HC00
1/2 IC5
74HC00
new resistor
(protection when
probing)
avoids spectaculer
short of +5V to 0V
if pins 5 and 6
are bridged by
careless probe
UNUSED SECTION
OF IC5
IC4
IC5
PCB FILED AS LB1KPD
Capacitors absorb any
decoder glitch, although
software uses RADD3 to U2 pin 6
to disable U2 while addresses change
Board 9/12/94
as supplied had
U2 pins 4,5 to 0V
pin 6 to RADD3 (=0V)
U3 pins 4, 5 to 0V and
RADD3 pin 6 to 5V
File: LB1KPD_2.SCH
Started: 960229
980205
Last Edit: 960229
990419
Drawn by:
2D35 0J25 0D40
E & T S
E&TS Lottery Controller Keypad Matrix
Interface Connector
(c) 1998 E & TS
Sheet 2/5
..\Clients\ETS\ETS_LB1\Kpd_LB1\



Notes

① 1,2,3,4,5,6,7,8,9,*,0,# are "Alps" type tactile pushbuttons as are any on-board pushbuttons

② Keyswitch K is the keyswitch for gaining access to commands; it has been deleted 98 02/13, but provision is made here in case it is reinstated.

③ Keyswitch C is the summer/winter time switch, @ 98 02/13 it is to be a toggle switch near the printer, or deleted altogether.

④ "Spare" is optional.

⑤ Red, Yellow, Green, Print, Cancel are all off board pushbuttons Positions for duplicates on-board are shown here, so that they may be installed for testing/development

PCB FILED AS LB1KPD

File:	LB2KPD_3.SCH
Started:	980205
Last Edit:	960229 990419
Drawn by:	0D56 0J10 0D55

E & T S

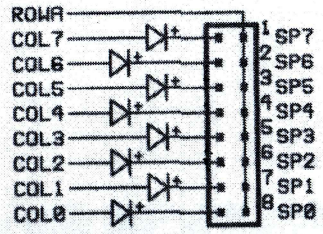
E&TS Lottery Controller Keypad Matrix

Keypad Pushbuttons

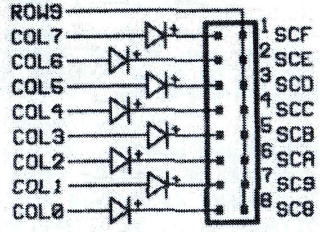
(c) 1998 E & TS

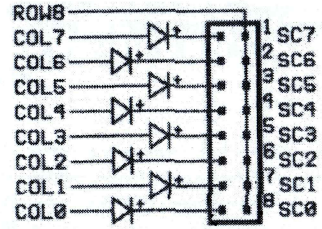
Sheet 3/4

..\Clients\ETS\ETS_LB1\Kpd_LB1\



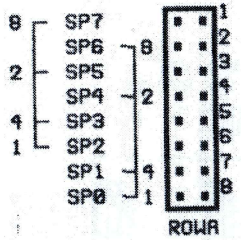
SPARE (UNUSED)



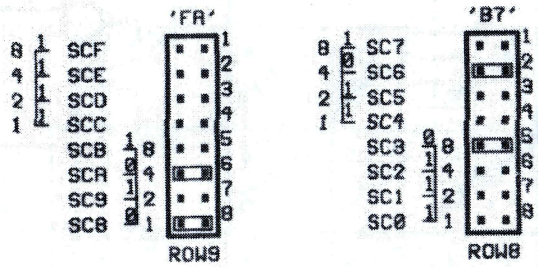


LINKS TO SET SITE CODE

SPARE



eg SITE CODE 'FA87'



8421 1111 'F'
8421 1010 'A'
8421 1011 'B'
8421 0111 '7'

LINK FITTED = '0' (LOW)
LINK NOT FITTED = '1' (HIGH)

PCB FILED AS LB1KPD

..\Clients\ETS\ETS_LB1\Kpd_LB1\

File: LB2KPD_4.SCH	E & T S
Started: 960229 980205	E&TS Lottery Controller Keypad Matrix
Last Edit: 960229 990419	Site Code, Spare Links
Drawn by: 12D10 0D06 0D25	(c) 1998 E & TS — Sheet 4/4